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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,070	12/20/2001	Robert Kaiser	W&B-INF-952	9447

24131 7590 06/10/2004

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,070	KAISER ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-22 are presented for examination.

Priority

The examiner acknowledges the applicant's claim for priority date of 12/20/2000.

Information Disclosure Statement

The examiner has considered the applicant's Information Disclosure Statement.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 4 recites the limitation "said processing unit" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim.

2. Claim 9 recites the limitation "said processing unit" in line 3. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 10 recites the limitation "said processing unit" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 12 recites the limitation "the group" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 15 recites the limitation "the processing unit" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 12 are rejected under 35 U.S.C. 103(b) as being anticipated by Dreibelbis et al., "Processor-Based Built-In Self-Test for Embedded DRAM". Dreibelbis et al. teaches an integrated circuit and methodology (see Abstract), comprising: a data processing unit (page 1732 column 1 paragraph 3, and column 2 paragraph 1); a buffer memory having registers for storing data for said data processing unit (FIG.2 Redundancy Allocation Register, and FIG.6(a) and (d), said buffer memory connected to said data processing unit (FIG.2 via Clock Generator). The data in this buffer is serially passed on (see Abstract), to be used by the circuit in determining which fuses are blown in repair of the memory.(page 1732 paragraph 3). Dreibelbis et al. further teaches a setting memory (FIG.6 Failing Word Address Reg, and page 1736 column 2 paragraph 2) connected to the buffer memory (FIG.6 Failed Word Address Counter), the setting memory at least one of being written to (page 1736 column 2 paragraph 2) and being read from through said buffer memory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-3 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreibelbis et al., "Processor-Based Built-In Self-Test for Embedded DRAM", and in view of Tsukakoshi et al., U.S. Patent No. 5337318.

As per Claims 2 and 13:

Dreibelbis et al. fails to further teach the integrated circuit and method according to claim 1 or 12, including circuit elements, said setting memory activating said circuit elements. However, in the analogous art of Tsukakashi et al., a setting memory (column 6 lines 39-40) activates redundant memory elements (column 4 lines 55-68 and column 5 lines 1-10). The advantage stated for this device is recited in column 1 lines 64-68 and column 2 lines 1-38 as being a way to quickly test for defective memory cells using several setting memories. One with ordinary skill in the art at the time of the invention would be motivated as suggested by Tsukakoshi et al. to combine the multiple setting memories of Tsukakoshi et al. with the system of Dreibelbis et al. in order to more quickly complete the testing of LSI memories.

As per Claims 3 and 14:

Tsukakoshi et al. further teaches the integrated circuit and method according to claim 2 or 13, including a memory having memory areas (column 1 lines 1-10), said circuit elements being memory elements used to replace at least one of said memory areas (see Abstract). And in view of the motivation previously stated in Claim 2 or 13, the claims are rejected.

8. Claims 4-10 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreibelbis et al., "Processor-Based Built-In Self-Test for Embedded DRAM".

As per Claims 4 and 15:

The integrated circuit or method according to claim 1 or 12, is further limited wherein said processing unit has an arithmetic logic unit. Although the processor of Dreibelbis et al. does not specifically recite an ALU, ALUs are well known components of microprocessors. And one with ordinary skill in the art at the time of the invention, motivated by Dreibelbis et al. (Abstract) to provide powerful DRAM testing with minimum I/O pins by utilizing a processor, would have found it obvious to also have provided an ALU with the processor.

As per Claims 5 and 16:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 4 or 15, wherein a register of said registers processes data (FIG.4 bits 0-31); and another register of said registers processes coded instructions for said arithmetic logic unit (FIG.4 bits 32-33). And in view of the motivation previously stated, the claims are rejected.

As per Claims 6 and 17:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 5 or 16, wherein said buffer memory (FIG.6 (a) and (d)) is two buffer memories each containing data to be processed. And in view of the motivation previously stated, the claims are rejected.

As per Claims 7 and 18:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 1 or 12, wherein said buffer memory is a latch (FIG.6 (d) Failed Word Address Counter). It is well known in the art that when a counter is not counting, it is a latch that holds the count. And in view of the motivation previously stated, the claims are rejected.

As per Claims 8 and 19:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 1 or 12, wherein said buffer memory has a shift register (FIG.6 (a) scan in and scan out of Redundancy Allocation Registers). It is well known in the art that when a register scans in and out, it does so by means of a shift register. And in view of the motivation previously stated, the claims are rejected.

As per Claims 9 and 20:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 8 or 19, wherein said shift register has at least one switch subdividing said shift register into registers for said processing unit. The two registers, Word Allocation and Bit Allocation are separate scanable registers and are switchable under control of Row

or Databit Commit (FIG.6 (a)). And in view of the motivation previously stated, the claims are rejected.

As per Claims 10 and 21:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 1 or 12, wherein said processing unit serially writes to and reads from each of said registers (FIG.2 between Sequencer and Redundancy Allocation, and see "Clock Generator" on page 1734). And in view of the motivation previously stated, the claims are rejected.

9. Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreibelbis et al., "Processor-Based Built-In Self-Test for Embedded DRAM", and in view of Nakahara et al., U.S. Patent No. 6445627. The integrated circuit or method according to claim 1 or 12 is further limited in that the said setting memory has electrical fuses, but Dreibelbis et al. does not specifically teach this feature. However, an analogous art, Nakahara et al. does recite this feature. The setting circuit (see Abstract) of Nakahara et al. controls the blowing of electrical fuses (FIG.3 and FIG.5). And, advantages cited by Nakahara et al. is a setting circuit that reduces I/O lines and circuit overhead with reduced cost (column 1 lines 35-67 and column 2 lines 1-67, and column 3 lines 1-63). One with motivation as suggested by Nakahara et al., and with ordinary skill in the art at the time of the invention, would find it obvious to use the setting circuit of Dreibelbis et al. to blow fuses within the circuit proposed by Nakahara et al., and so the claims are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Albert DeCady
Primary Examiner